Amendments to the Claims:

Claim 1 has been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Please cancel claims 19, 20 and 26 through 29 without prejudice or disclaimer.

1. (Currently amended) A method of forming a semiconductor device, comprising:

providing a semiconductor substrate having an active surface including at least one layer of integrated circuitry thereon, said active surface defining a plurality of individual die locations thereon, and a plurality of bond pads associated with each of said plurality of individual die locations;

forming at least one intermediate conductive element on at least one bond pad of said plurality of bond pads;

forming a pattern of mutually transverse channels in said active surface to a depth below said at least one layer of integrated circuitry, said channels circumscribing a semiconductor element location comprised of at least one individual die and exposing peripheral edges of said at least one layer of integrated circuitry; and

forming a layer of encapsulant material over substantially all of said active surface and into said channels such that a surface of said layer of encapsulant material has a pattern of depressions over said channels and a portion of said at least one intermediate conductive element is exposed through and coplanar with said surface of said layer of ~~encaplsulant~~ encapsulant material.

2. (Previously presented) The method of claim 1, further comprising forming at least one external conductive element over said exposed portion of said at least one intermediate conductive element.

3. (Previously presented) The method of claim 1, further comprising severing said semiconductor substrate along said pattern of depressions over said channels into a plurality of semiconductor elements, each semiconductor element comprised of at least one individual die location, wherein said exposed peripheral edges of said at least one layer of integrated circuitry remain covered with said encapsulant material.

4. (Original) The method of claim 1, further comprising forming said channels with sloped side walls defining opposing chamfers.

5. (Canceled)

6. (Original) The method of claim 1, further comprising forming said channels with substantially parallel side walls.

7-10. (Canceled)

11. (Previously presented) The method of claim 1, wherein forming said at least one intermediate conductive element is effected by forming at least one solder ball.

12. (Previously presented) The method of claim 1, wherein forming said at least one intermediate conductive element is effected by forming at least one pillar of a conductive or conductor-filled epoxy or a metal-filled elastomer.

13. (Previously presented) The method of claim 1, wherein forming said at least one intermediate conductive element is effected by a wire bonding capillary.

14. (Previously presented) The method of claim 2, wherein forming said at least one external conductive element comprises forming at least one solder ball.

15. (Previously presented) The method of claim 2, wherein forming said at least one external conductive element comprises forming at least one pillar of a conductive or conductor-filled epoxy.

16. (Previously presented) The method of claim 2, wherein forming said at least one external conductive element comprises applying an anisotropically conductive film over said encapsulant material.

17. (Previously presented) The method of claim 1, further comprising forming said layer of encapsulant material from a material selected from the group comprising filled polymers, epoxies, silicones, silicone-carbon resins, polyimides, polyurethanes and glasses.

18. (Previously presented) The method of claim 1, further comprising forming another layer of encapsulant material on a back side of said semiconductor substrate.

19-20. (Canceled)

21. (Previously presented) The method according to claim 3, comprising:

placing at least one of said plurality of semiconductor elements with said at least one intermediate conductive element in alignment with at least one conductive bump protruding from a carrier substrate; and

electrically connecting said at least one intermediate conductive element and said at least one conductive bump.

22. (Previously presented) The method of claim 21, further including forming at least one bond pad over said exposed portion of said at least one intermediate conductive element before electrically connecting said at least one intermediate conductive element to said at least one conductive bump.

23. (Previously presented) The method of claim 2, further comprising severing said semiconductor substrate along said pattern of depressions over said channels into a plurality of semiconductor elements, each semiconductor element comprised of at least one individual die location, wherein said exposed peripheral edges of said at least one layer of integrated circuitry remain covered with said encapsulant material.

24. (Previously presented) The method of claim 23, comprising:

placing at least one of said plurality of semiconductor elements with said at least one external conductive element in alignment with at least one terminal pad of a carrier substrate; and

electrically connecting said at least one external conductive element and said at least one terminal pad.

25. (Withdrawn) The method of claim 2, further comprising placing said semiconductor substrate with said external conductive elements in alignment with terminal pads of a carrier substrate and electrically connecting said external conductive elements to said terminal pads.

26-29. (Canceled)

Amendments to the Drawings:

The attached sheets of drawings include changes to FIGS. 1C-1E and 2. These sheets, which include FIGS. 1A-5, 7A and 7B replace the original sheets including FIGS. 1A-5, 7A and 7B. FIGS. 1C-1E have been amended to include broken lines designating depressions 29 and reference designators have been added to FIGS. 1C-1E and 2 to point out these features.

Attachment: Replacement Sheets (2)
Annotated Sheets Showing Changes (2)